



2/13

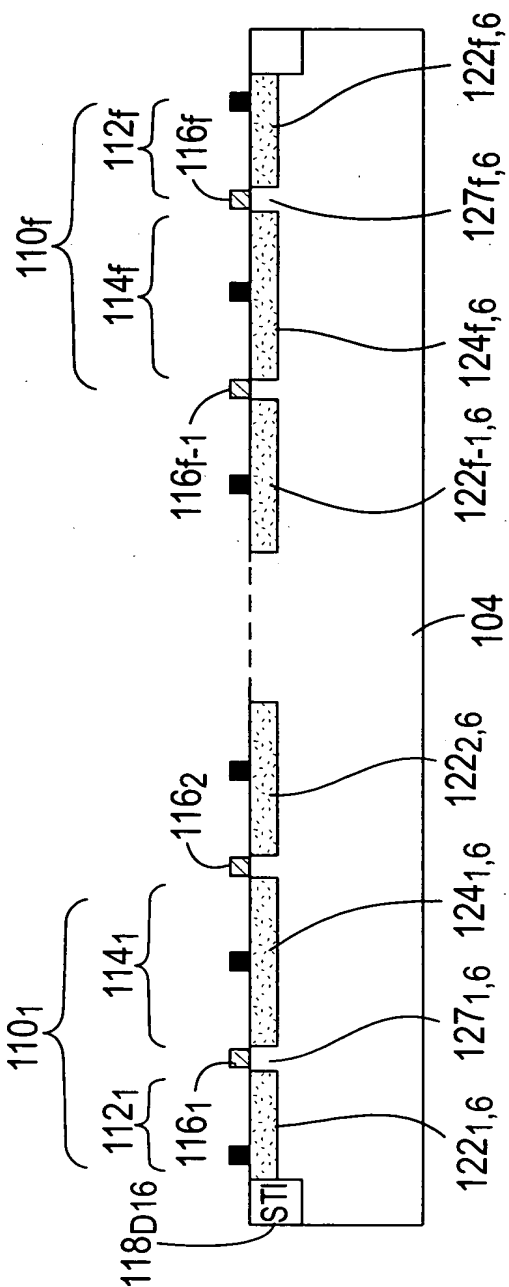


FIG. 2A

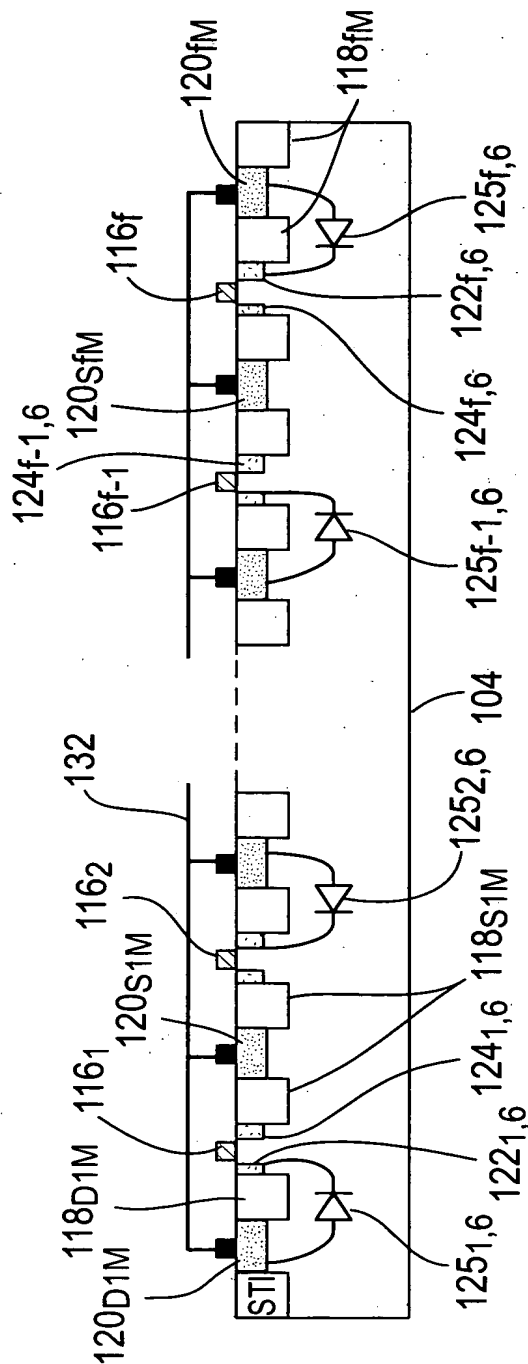


FIG. 2B

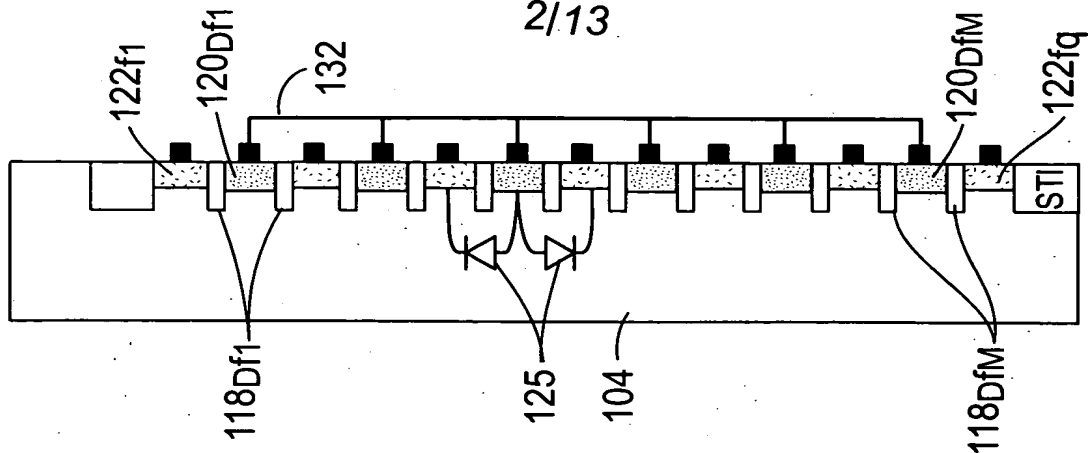


FIG. 2C

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FIG. 3

The diagram illustrates an ESD protection circuit for a PMOS driver. The circuit is connected to a power supply rail V_{DD} and a signal rail V_{DDX} . A PMOS DRIVER (700) is connected to V_{DDX} and a PAD (20). The PAD is connected to an ESD DETECTOR (310) and an NMOS CLAMP OR SELF-PROTECTING OUTPUT DRIVER (100). The ESD DETECTOR (310) is connected to a TRANSFER CIRCUIT (320), which is connected to a VOLTAGE LIMITER (330). The VOLTAGE LIMITER (330) is connected to a PRE-DRIVER (600) and a PRE-DRIVER CONTROL (500). The PRE-DRIVER (600) is connected to the NMOS CLAMP OR SELF-PROTECTING OUTPUT DRIVER (100). The NMOS CLAMP OR SELF-PROTECTING OUTPUT DRIVER (100) is connected to the PAD (20) and a GND (15). The circuit includes several capacitors: C_{DD} (900) connected to V_{DD} , C_{DDX} (901) connected to V_{DDX} , and C_{DD} (90) connected to the PAD (20). The circuit also includes resistors 800 and 801 connected to the GND (15) rail.

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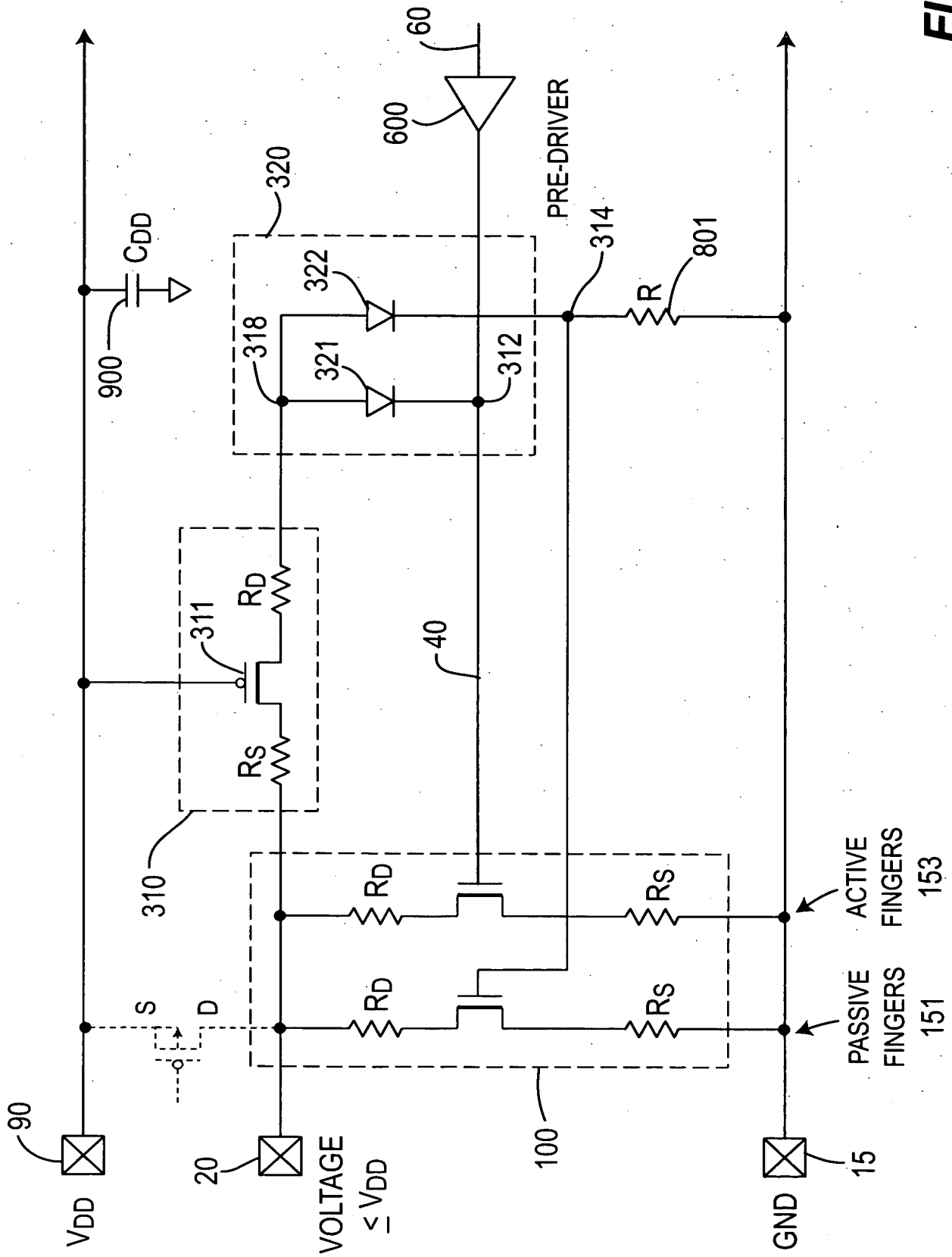
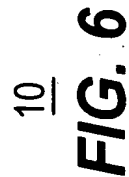


FIG. 4

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FIG. 7

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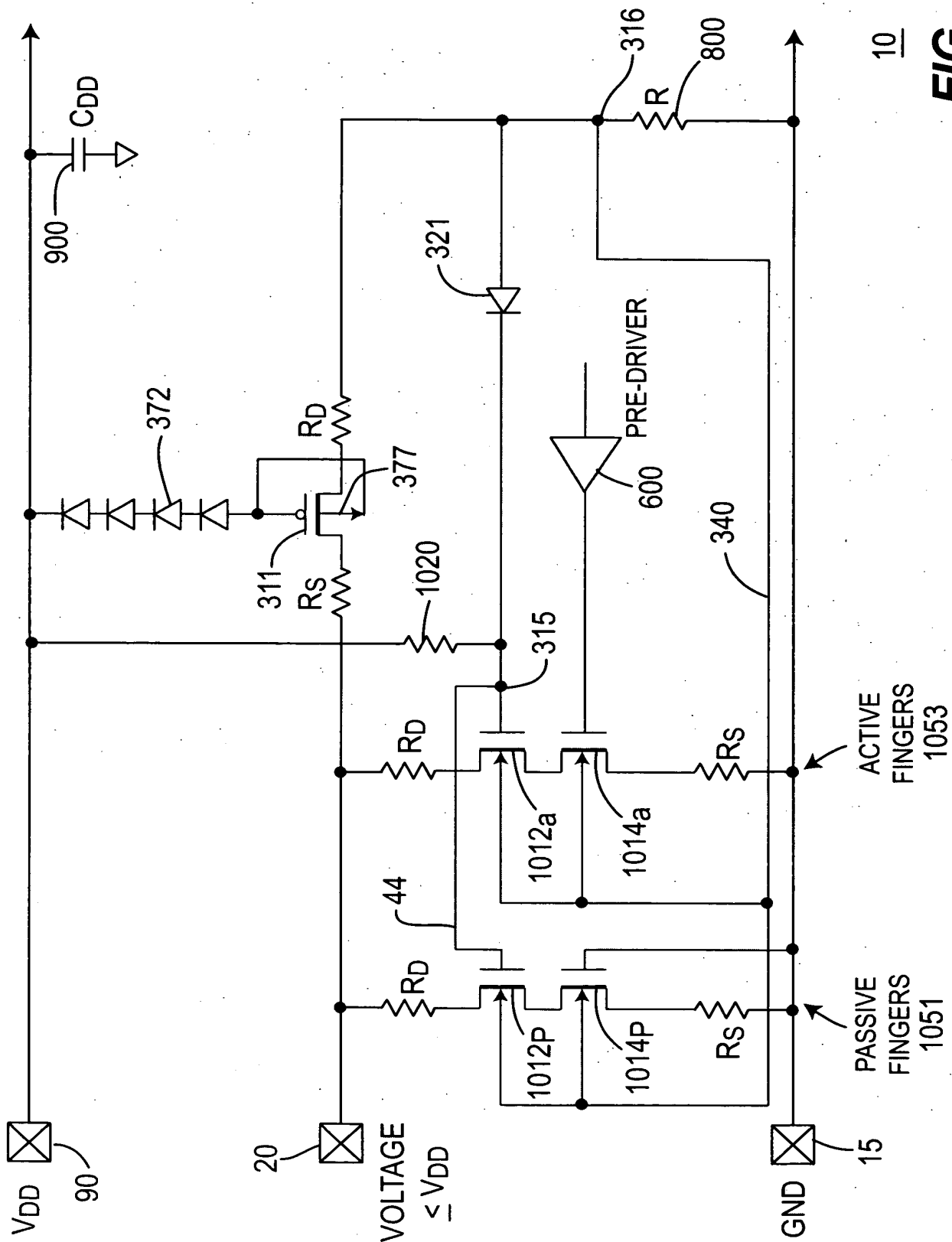


FIG. 8

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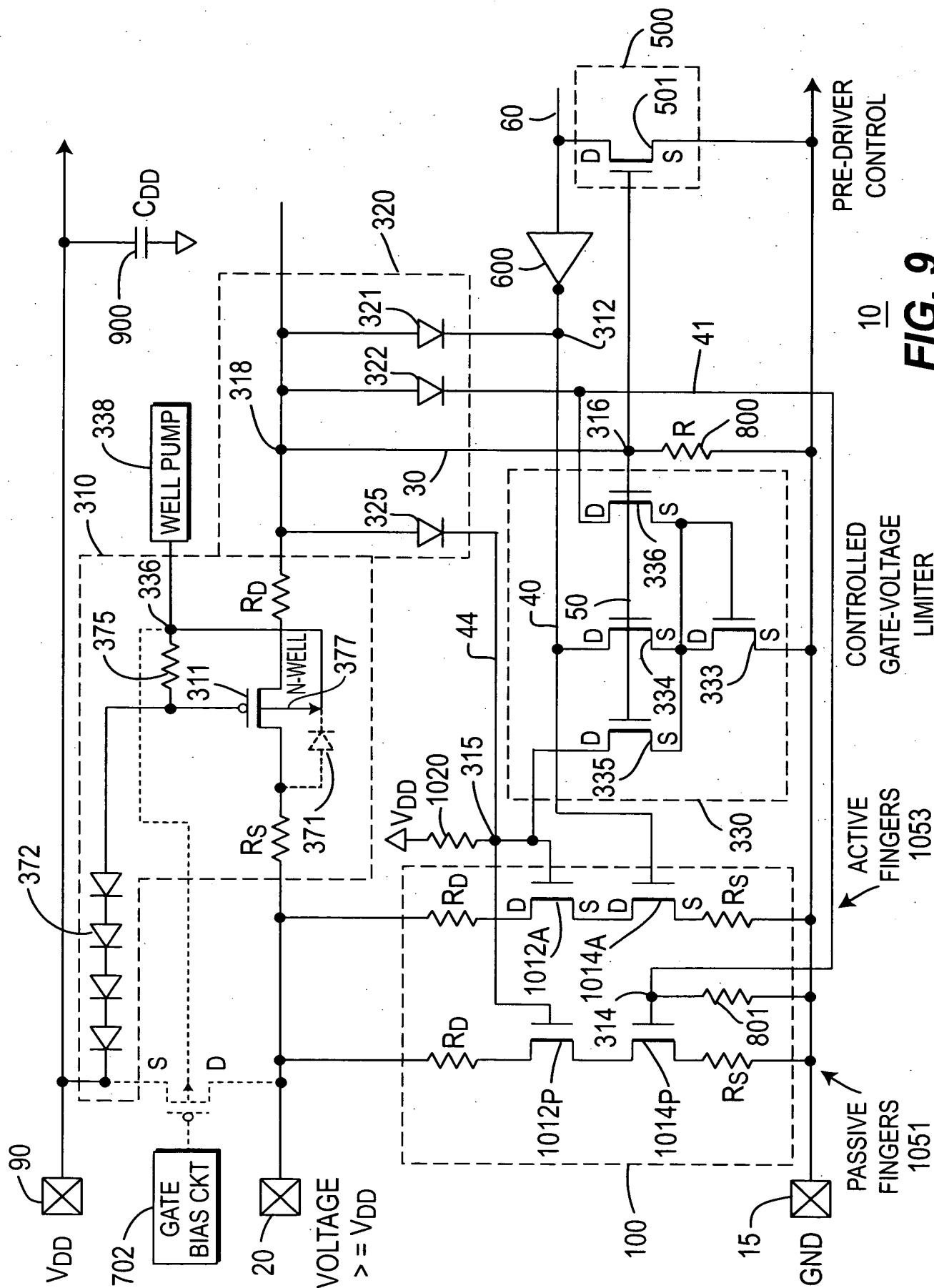


FIG. 9

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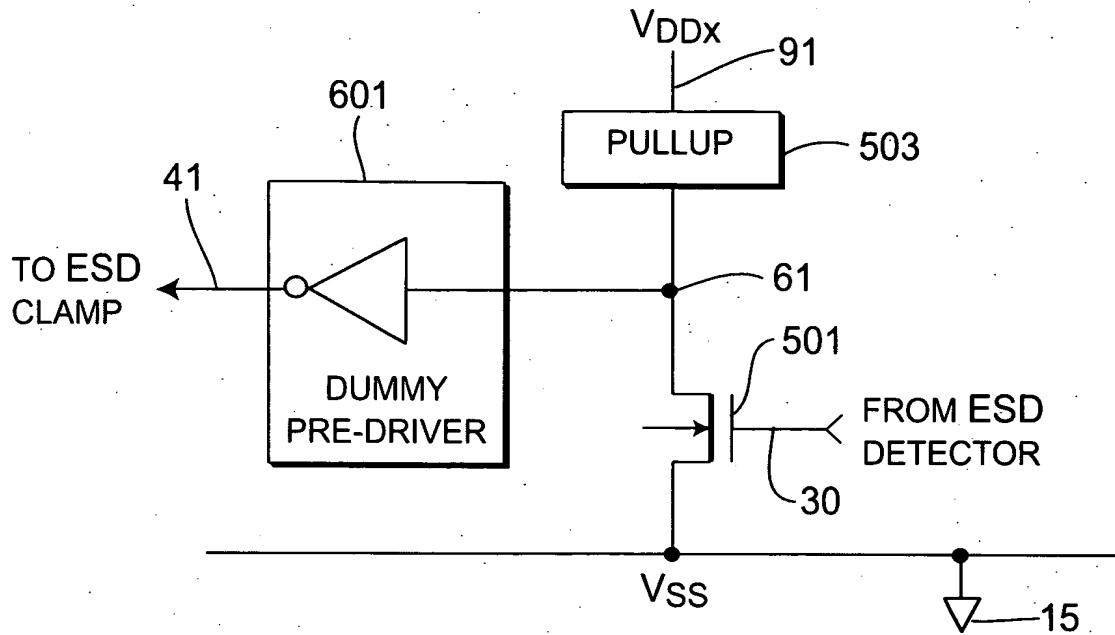


FIG. 11

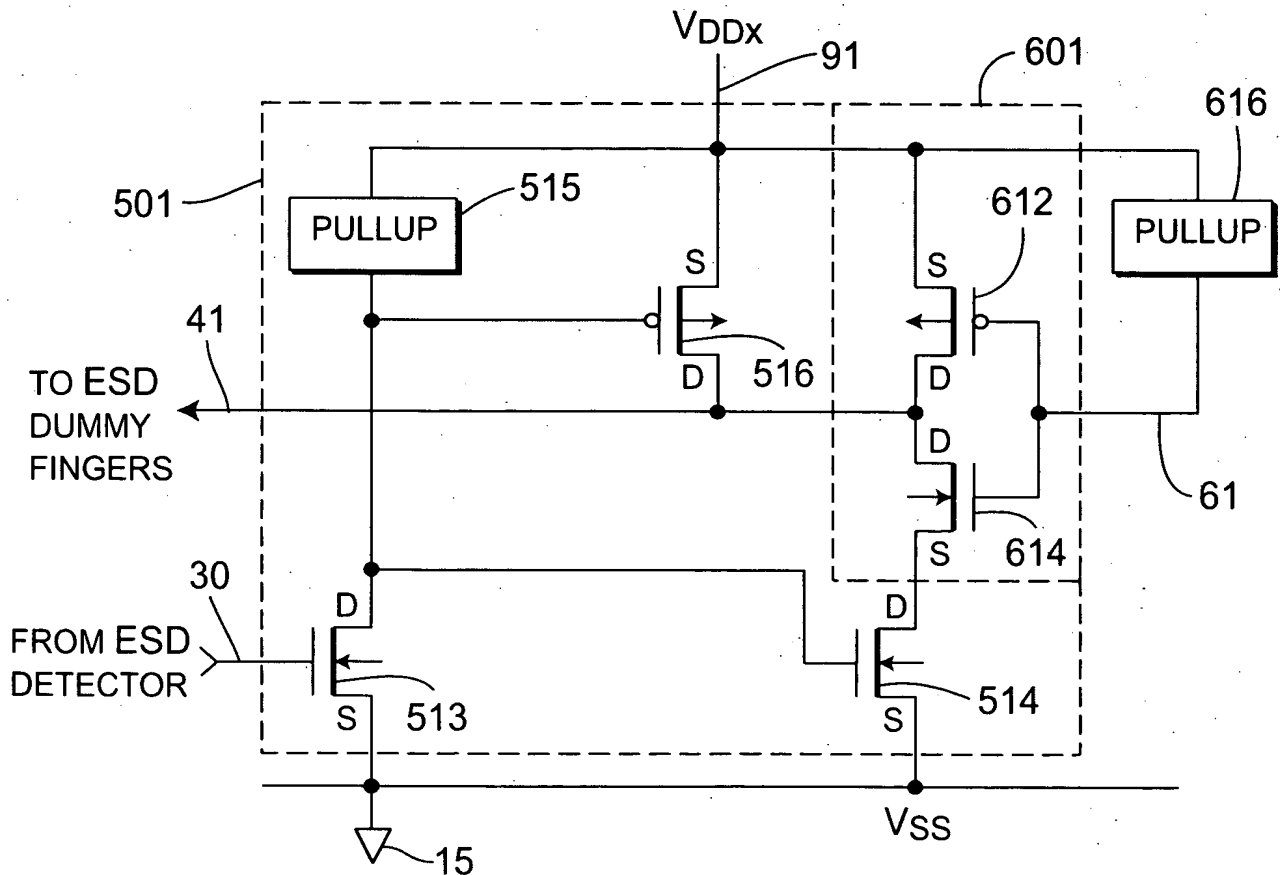


FIG. 12A

FIG. 12B

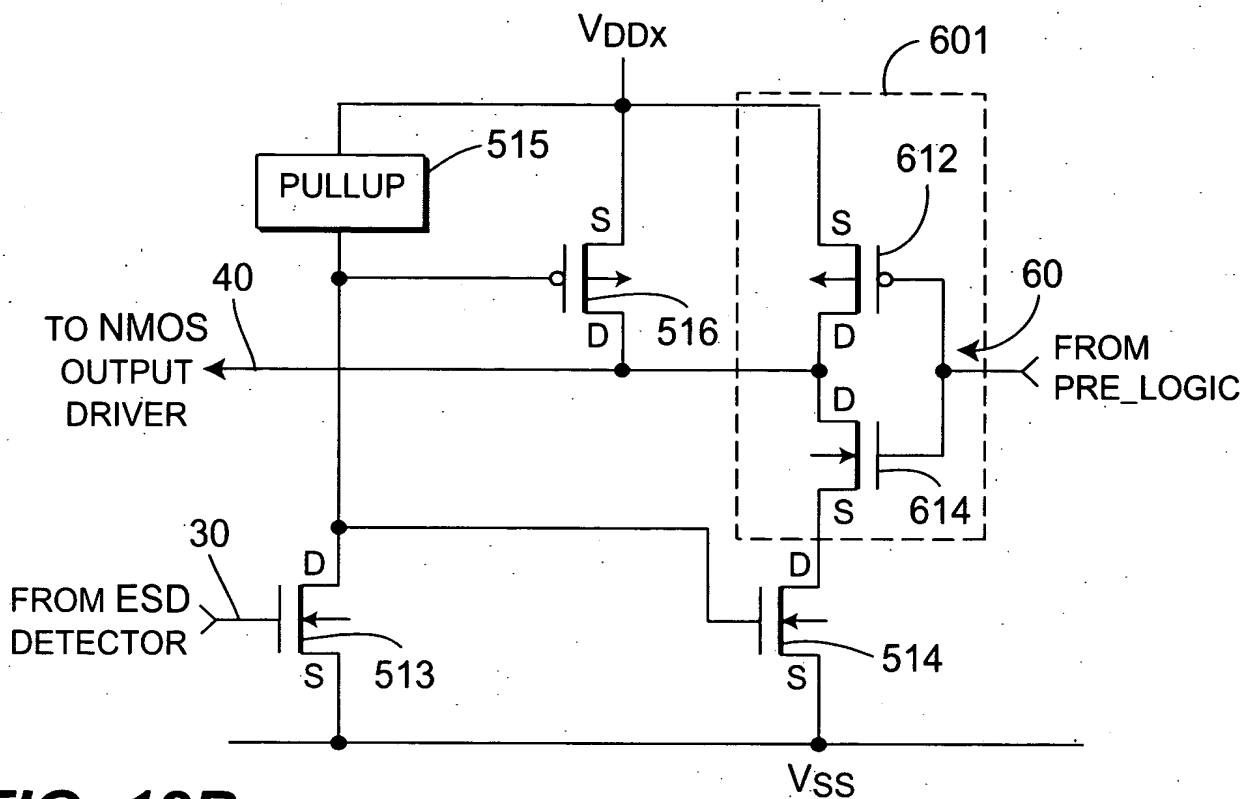


FIG. 12C

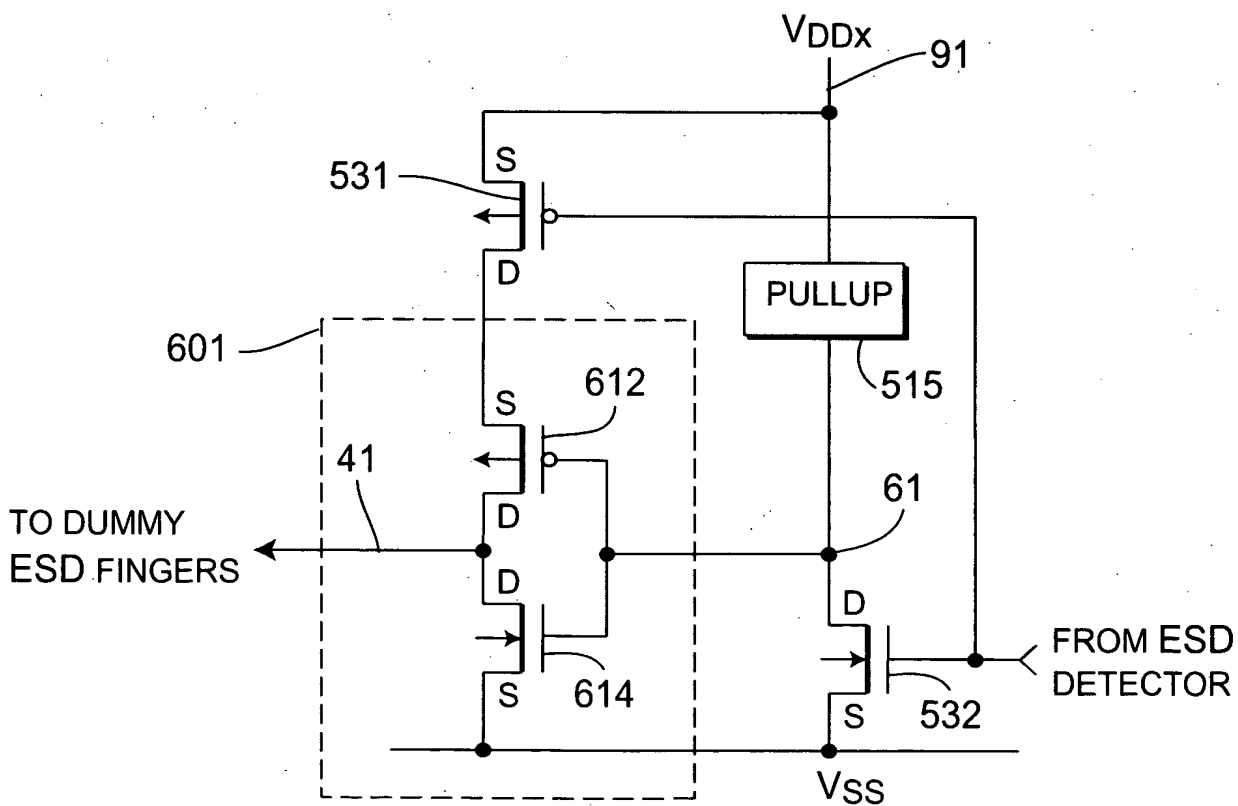




FIG. 13

